reference to Fig. 5. A clock signal having about 48 MHz frequency (a first frequency) is supplied to DSP 2 from interface LSI 52. When analog image signal S_P is supplied from camera sensor 61 to DSP 62 as shown in Fig. 5, ADC 72, shown in Fig. 4, converts analog image signal S_P into digital image data D_{P0} with 8 bits per pixel. In this example, since camera sensor 11 records with resolution of 1280 x 960 pixels, one pixel being 8 bits per pixel, its data amounts to1,228,800 bits. The above image data D_{P0} is subjected to image processing, such as white balancing, exposure-gain adjustment, etc., in adjusting circuit 73, and the processed image data are subsequently stored directly in external RAM 63 as image data D_{P1}, that is controlled by external RAM controller 74, for buffering. The path in which this sequence of processing is performed is called still image process path. In this case, external RAM 63 may be configured as having a double buffering structure composed of one-sided memory area 63_a and two-sided memory area 63_b, as shown in Fig. 5, for example, to enable time losses in the image processing to be recovered.

Furthermore, the above image data D_{P1} are also supplied to RSPB 76 in order to use main LC panel 54 and sub LC panel 55 as camera finders and display image data D_{P1} on the camera finders. Specifically, RSPB 76 performs resizing processing to resize image data D_{P1} with 8 bits per pixel and 1280 x 960 pixels per frame into image data D_{P3} with 8 bits per pixel and 320 x 240 pixels per frame, and then delivers the resized image data D_{P3} to FTB 77. FTB 77 then converts image data D_{P3} composed of red data R, green data G and blue data B that are image data in RGB format into image data D_{p4} composed of luminance data Y, color difference data U and V that are image data in YUV format to supply image data D_{p4} to interface LSI 52 via 16-bit-wide bus 79. Image data D_{p4} are then supplied to main LC panel 54 or sub LC panel 55 through interface LSI 52 for display thereon. The process in which the above sequence of processing is performed is called a camera-finder path.

In the meantime, during a vacant time period in which no process is performed in the camera-finder path, encoder 74 operates on about 12 MHz clock signal, performs compression-coding processing on image data D_{P1} read from external RAM 63 under the control of external RAM controller 73, to convert image data D_{P1} into image data D_{P2} in JPEG format in a time division manner using internal RAM 75 as a compression-coding processing buffer, and stores image data D_{P2} in an unoccupied area of external RAM 63. The above process is typically designed to enable one frame of still image data to be compression-coded during a vacant time period in which 3-frame image data are processed in the camera-finder path. If the compression-coding processing cannot be performed with the above timing, the clock signal with about 12 MHz frequency may be multiplied using a PLL (Phase Locked Loop).

When the above compression-coding processing is completed, the completion is notified to interface LSI 52 and further to CPU 53. With this notification, CPU 53 can capture image data D_{P2} stored in external RAM 63 through register 80 that constitutes interface 52 at required time, thereby realizing distributed processing. Moreover, the load of CPU 53 is reduced because CPU53 has no relation to image data D_{P4} for a camera finder.

Operation in the mobile camera mode will next be described with reference to Fig. 6. In this mode, the power source for external RAM 63 is switched off to place external RAM 63 in an inactive state. The broken line of external RAM 63 in Fig.6 represents its inactive state. When analog picture signal S_p is supplied from camera sensor 61 to DSP 62, to which a clock signal with about 12 MHz frequency (a second frequency) is supplied from interface

LSI 52 as shown in Fig. 6, ADC 72 shown in Fig. 4 converts analog picture signal S_p into digital image data D_{P0} with 8 bits per pixel. The above digital image data D_{P0} is subjected to image processing, such as white balancing, exposure-gain adjustment, etc., in adjusting circuit 73. The processed image data is buffered in internal RAM 75 for compression-coding as image data D_{P1}, and delivered to RSPB 76. In response, RSPB 76 performs resizing process on the above-described image data D_{P1} to resize image data D_{P1} with 8 bits per pixel and 1280 x 960 pixels per frame into image data D_{P3} with 8 bits per pixel and 320 x 240 pixels per frame, stores the image data D_{P3} in internal RAM 75 for buffering, and supplies the image data to FTB 77. FTB 77 then converts image data D_{P3} composed of red data R, green data G and blue data B, that are image data in RGB format, into image data D_{p4} composed of luminance data Y, color difference data U and V, that are image data in YUV format, and supplies the image data D_{p4} to interface LSI 52 via 16-bit-wide bus 79. The image data D_{p4} is then supplied to main LC panel 54 or sub LC panel 55 through interface LSI 52 for display thereon. The process path in which the above sequence of processing is performed is called a camera-finder path.

In the meantime, during a vacant time period in which no process is performed in the camera-finder path, encoder 74 operates on about 12 MHz clock signal, performs compression-coding processing on image data D_{P1} read from the other area of internal RAM 75, to convert image data D_{P1} into image data D_{P2} in JPEG format in a time-division manner using internal RAM 75 as a compression coding buffer, and stores image data D_{P2} in an unoccupied area of internal RAM 75. The above process is usually set in advance to correspond to three frames of the process in the camera-finder path, and is thus designed to enable still image data of one frame to be processed for a time period during